Listing of the Claims

1. (original) A method for forming a recessed gate structure with reduced current leakage and overlap capacitance comprising the steps of:

providing a silicon substrate including one of N and P-well doped regions and an overlying the CVD silicon oxide layer;

forming an opening in the CVD silicon oxide layer to include a recessed area extending into a thickness portion of the silicon substrate;

thermally growing a gate oxide over exposed silicon substrate portions of the recessed area;

backfilling the opening with polysilicon;

planarizing the polysilicon to the opening level to reveal the silicon oxide layer; and,

selectively removing the silicon oxide layer to form a recessed gate structure.

2. (original) The method of claim 1, further including steps following the step of forming an opening and prior to the step of thermally growing a gate oxide comprising:

thermally growing a first silicon oxide layer to line the recessed area;

blanket depositing a silicon nitride layer over the opening to include lining the opening and overlying the first silicon oxide layer; and,

etching the silicon nitride layer and the first silicon oxide layer at a bottom portion of the opening to form exposed silicon substrate portions having a width smaller than the opening;

3. (original) The method of claim 1, wherein the recessed area is formed having a recessed depth of from about 200 Angstroms to about 400 Angstroms measured from the silicon substrate surface.

4. (original) The method of claim 1, further comprising the step of forming a source/drain extension (SDE) doped regions adjacent either side of the recessed gate structure.

5. (original) The method of claim 4, wherein the SDE doped regions are formed by one of an ion implant and a plasma immersion doping process.

6. (original) The method of claim 4, wherein the depth of the SDE doped regions measured from the silicon substrate surface to a lowermost portion of the SDE doped region is less than about 1200 Angstroms.

7. (original) The method of claim 6, wherein the depth of the recessed area is from about 1/3 to about 1/6 of the depth of the SDE doped regions.

8. (original) The method of claim 1, wherein the gate oxide layer thickness is less than about 50 Angstroms.

9. (original) The method of claim 2, wherein the first silicon oxide layer thickness is less than about 50 Angstroms.

10. (original) The method of claim 2, wherein the silicon nitride layer thickness is between about 50 Angstroms and about 200 Angstroms.

11. (original) The method of claim 2, wherein the step of etching comprises a dry anisotropic etching step for etching the silicon nitride layer.

12. (original) The method of claim 2, wherein the step of etching comprises a wet etching process for etching the first silicon oxide layer.

13. (original) The method of claim 1, further comprising the steps of forming sidewall spacers adjacent either side of the gate structure and forming source/drain (S/D) doped regions.

14. (original) The method of claim 13, further comprising the step of forming self aligned silicide (salicide) portions adjacent the sidewall spacers.

15. (withdrawn) A gate structure having reduced current leakage and overlap capacitance comprising:

a recessed area extending a first predetermined depth into an active portion of a silicon substrate comprising one of an N-well and P-well region;

a gate oxide layer lining at least a bottom portion of the recessed area;

a polysilicon portion overlying the gate oxide layer to extend above the surface of the silicon substrate to form a gate electrode portion; and

wherein source/drain extension (SDE) doped regions are disposed adjacent either side of the recessed area to a second predetermined depth greater than the first predetermined depth.

16. (withdrawn) The gate structure of claim 15, wherein the second predetermined depth is greater by a factor of at least about 3 compared to the first predetermined depth.

17. (withdrawn) The gate structure of claim 15, wherein the depth of the recessed area is from about 200 Angstroms to about 400 Angstroms.

18. (withdrawn) The gate structure of claim 15, wherein the lowermost portion of the SDE doped regions extends below the lowermost portion of the recessed area by less than about 1200 Angstroms.

19. (withdrawn) The gate structure of claim 15, further comprising a silicon oxide layer and an overlying silicon nitride layer lining the sidewalls of the recessed area disposed adjacent to a gate oxide layer covering a bottom portion of the recessed area.

20. (withdrawn) The gate structure of claim 15, wherein the gate oxide layer has a smaller width compared to the gate electrode portion.

21. (withdrawn) The gate structure of claim 15, wherein the gate oxide layer has a thickness less than about 50 Angstroms.

22. (withdrawn) The gate structure of claim 15, wherein the silicon oxide layer is less than about 50 Angstroms in thickness and the silicon nitride layer is from about 50 Angstroms to about 200 Angstroms in thickness.

23. (withdrawn) The gate structure of claim 15, further comprising sidewall spacers disposed adjacent either side of the gate structure.

24. (withdrawn) The gate structure of claim 15, further comprising self aligned silicide (salicide) portions disposed adjacent the sidewall spacers.

25. (withdrawn) A recessed gate structure having reduced current leakage and overlap capacitance comprising:

a recessed area extending a first predetermined depth into an active portion of a silicon substrate comprising one of an N-well and P-well region;

a gate oxide layer lining a portion of the bottom portion of the recessed area and an oxide/nitride layer lining the sidewalls of the recessed area;

a polysilicon portion having a larger width compared to the gate oxide layer width overlying the gate oxide layer to extend above the surface of the silicon substrate to form a gate electrode portion; and

wherein source/drain extension (SDE) doped regions are disposed adjacent either side of the recessed area to a second predetermined greater than the first predetermined depth.

26. (original) A method for forming a recessed gate structure having reduced current leakage and overlap capacitance comprising the steps of:

providing a silicon substrate including one of N and P-well doped regions and an overlying the CVD silicon oxide layer;

forming an opening in the CVD silicon oxide layer to include a recessed area extending into a thickness portion of the silicon substrate;

growing a first silicon oxide layer to line the recessed area;

blanket depositing a silicon nitride layer over the opening to include lining the opening and overlying the first silicon oxide layer;

etching the silicon nitride layer and the first silicon oxide layer at a bottom portion of the opening to form an exposed silicon substrate portion having a width smaller than the opening;

thermally growing a gate oxide over the exposed silicon substrate portion;

backfilling the opening with polysilicon;

planarizing the polysilicon to the opening level to reveal the silicon oxide layer;

selectively removing the silicon oxide layer to form a recessed gate structure; and,

forming Source/drain extension (SDE) doped regions adjacent either side of the recessed gate structure.